EPFL

Decoding FPGA Routing Architectures with NetCracker

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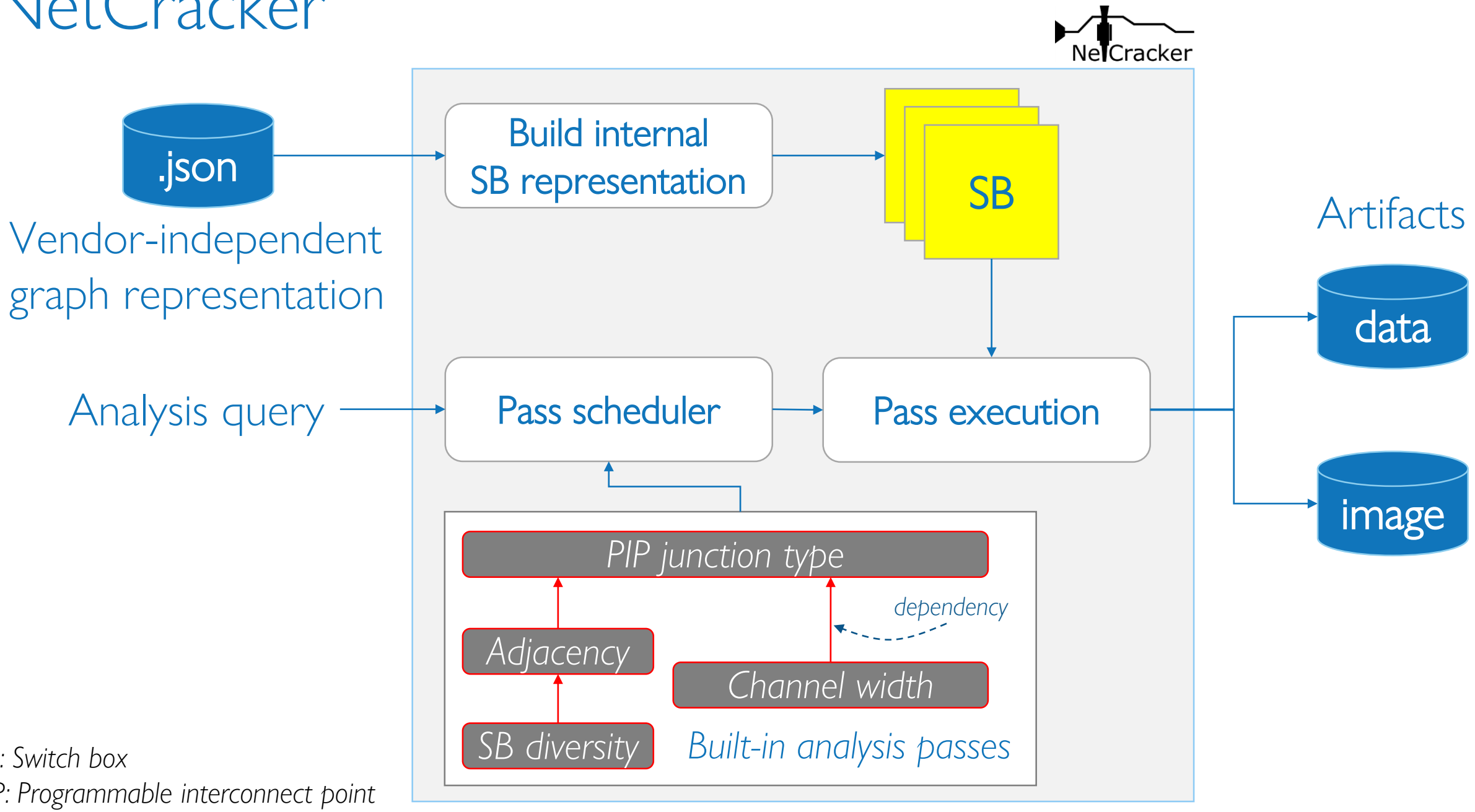
Why NetCracker?

- FPGA architectures are evolving
- Academic research can contribute to this development
- Understanding existing architectures is key
- NetCracker enables analysis of highly complex real routing architectures
- Identify research problems and incite future research
- Narrow the gap between academic research and industrial reality

NetCracker

Openly-available Python-tool for the analysis of FPGA routing architectures

NetCracker



SB: Switch box
PIP: Programmable interconnect point

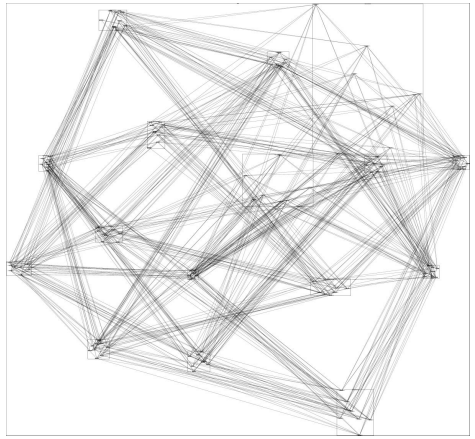
Outline

1. NetCracker
2. Applying NetCracker to AMD/Xilinx 7-Series family
   - Showcase the tool
     - Various analyses of routing architecture data readily available in design tools
     - Switch-box diversity
     - Routing channels
     - Connectivity analysis
   - Discuss results
     - Contrast with common knowledge and typical assumptions in academia

Insights are solely our own and should not be understood as factual

Switch-Box Diversity

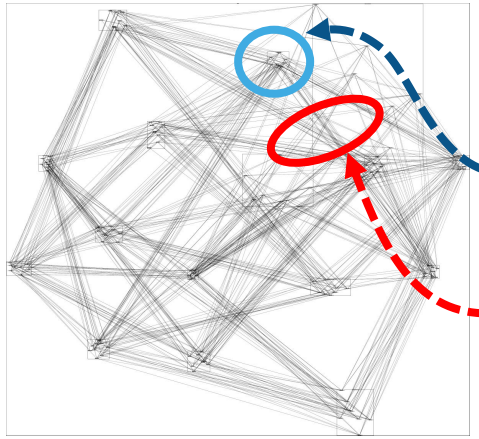
AMD/Xilinx Switch-Box Terminology



Switch-Box

- Routing switches
  - Programmable Interconnect Points (PIPs)
- Routing multiplexer
  - Collection of PIPs that drive a signal
- Switch-box (SB)
  - Collection of routing multiplexers
- Point of entry to or exit from an SB
  - PIP junction (PIPJ)

Switch-Box Graph View



Switch-Box

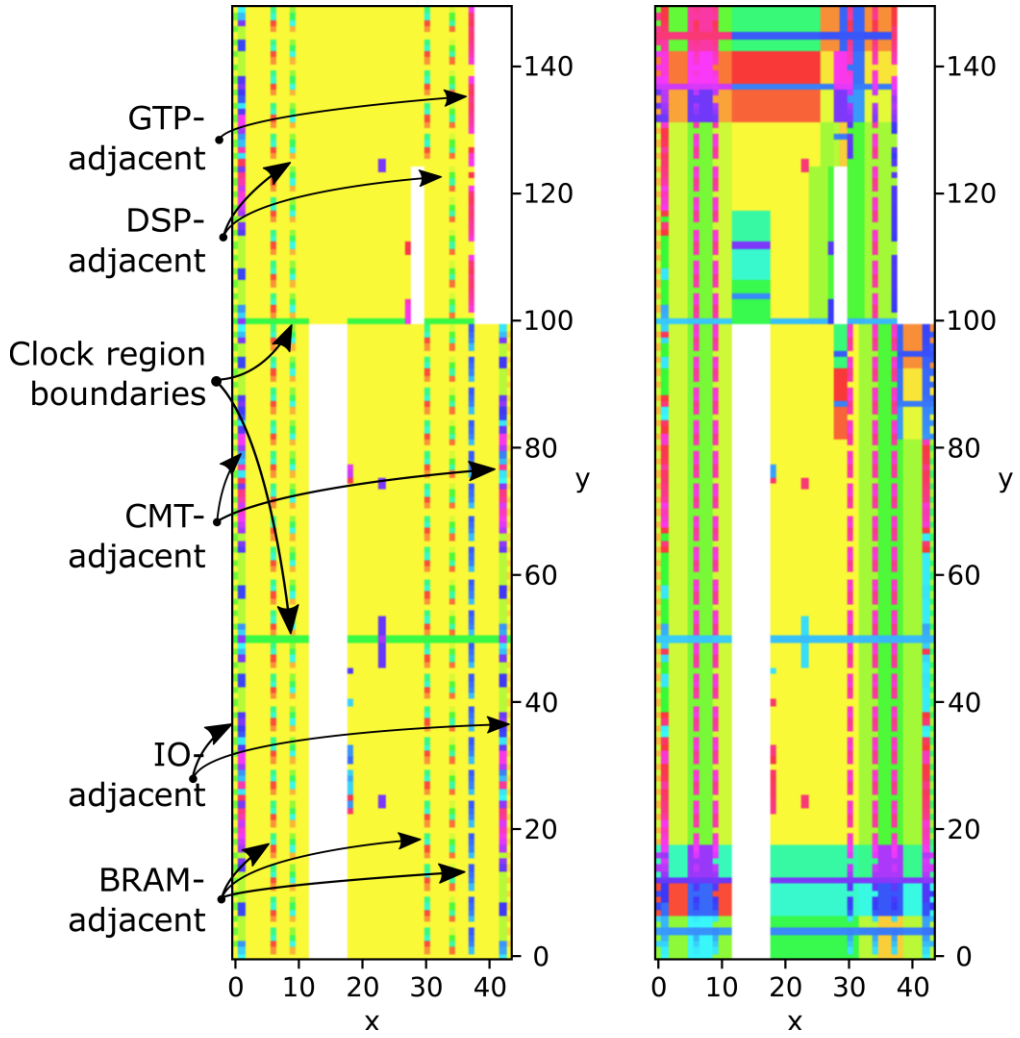
- Routing graph
  - Nodes: PIP junctions
  - Edges: Programmable connections

Switch-Box Diversity

High-level FPGA Architecture

Comparing SBs by their internal connectivity

Switch-Box Diversity

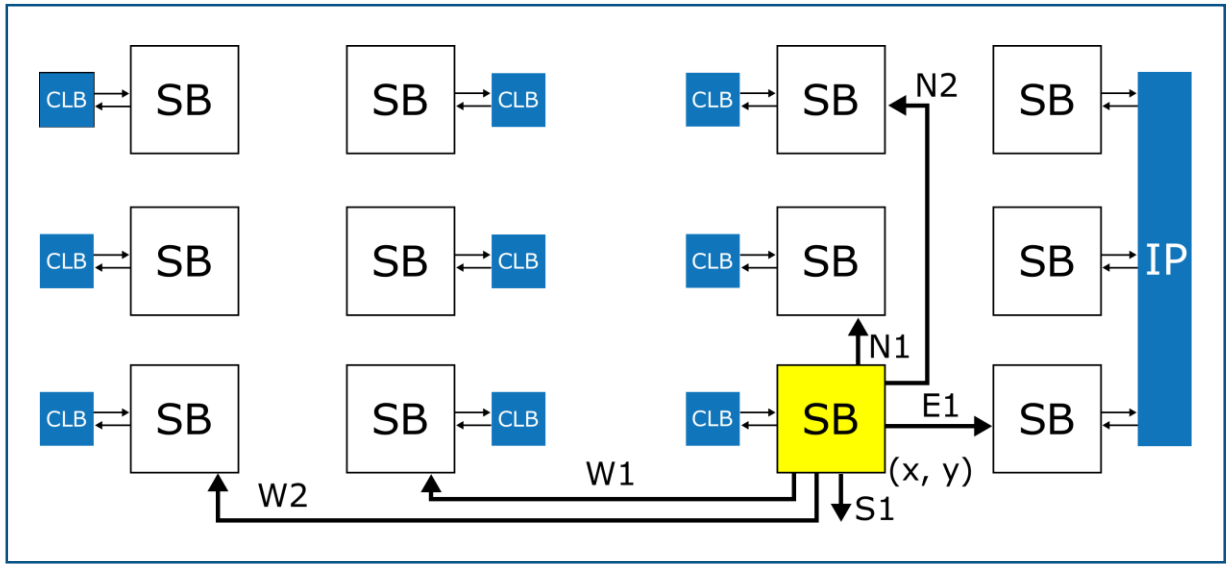


- Artix-7 XC7A35T
  - One color, one unique SB
  - In yellow, SBs interfacing CLBs
- Left, **excluding** connections to longs
  - Vertical uniformity
  - No wirelength-dependent patterns
- Right, **including** connections to longs
  - Diversity towards the edges

SBs interfacing configurable logic blocks are most often identical

Routing Channels

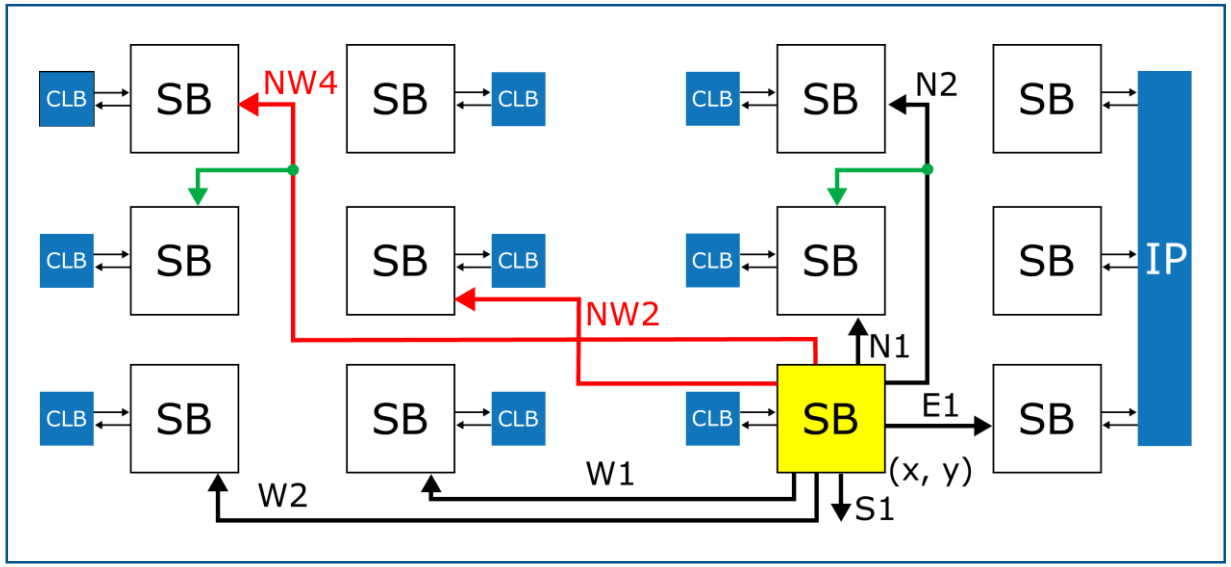
Routing Channels



- Cardinal wires
  - North, East, South, West
  - Example
    - E1: East, LEN-1
    - E1_BEG: Source PIPJ
    - E1_END: Destination PIPJ

PIPJ names match wire types

Routing Channels

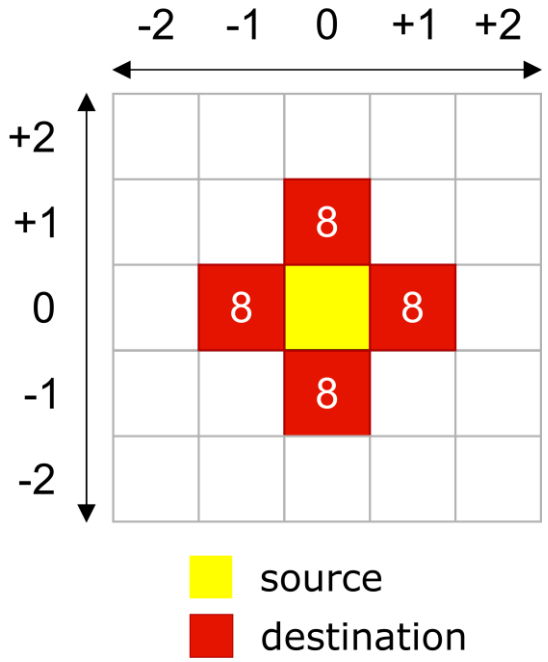


- Noncardinal (diagonal) wires
  - NE, NW, SE, SW
- Secondary destinations (stubs)
  - In green

Previously unknown diagonal wires with two destinations

Short-Range Connections

- Considering source PIPJ **name** only

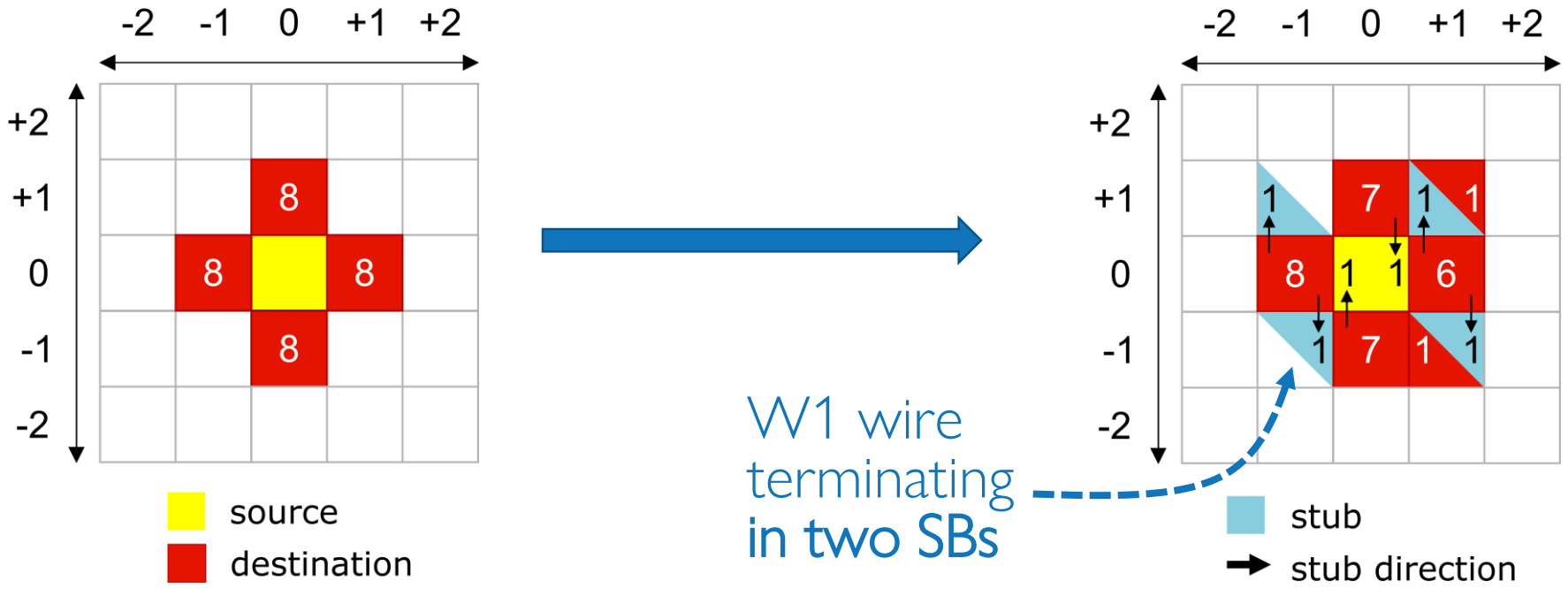


- In yellow, source SB
- In red, destination SB
- x-axis and y-axis:
  - **Offset** between the destination and source SB

Surprisingly high number of LEN-1 wires

Short-Range Connections

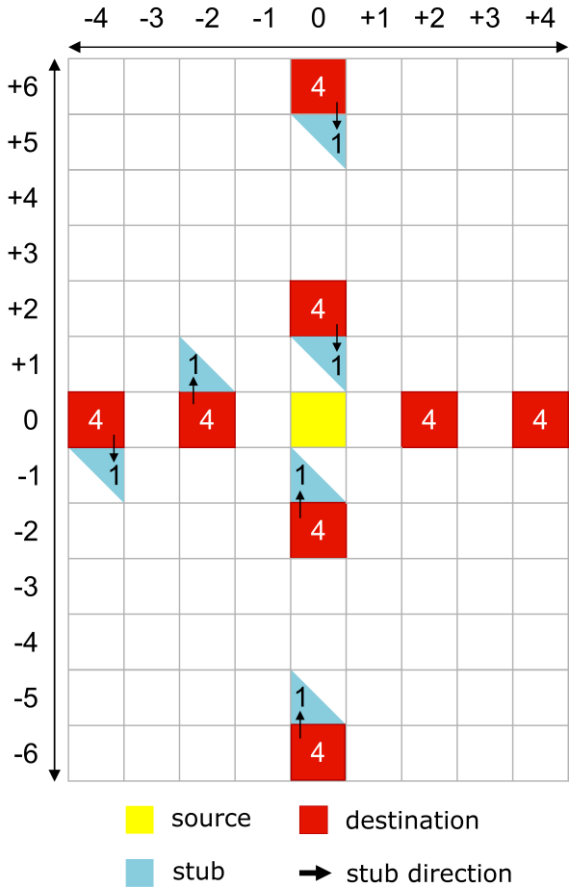
- Considering source PIPJ **name** only
- Considering destination PIPJ **location(s)**



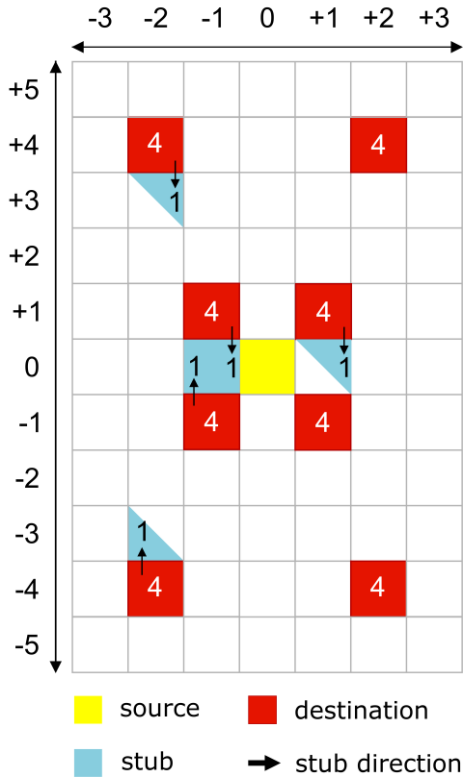
LEN-1 wires sometimes have secondary destinations

Mid-Range Connections

- Considering destination PIPJ location(s)
- Cardinal



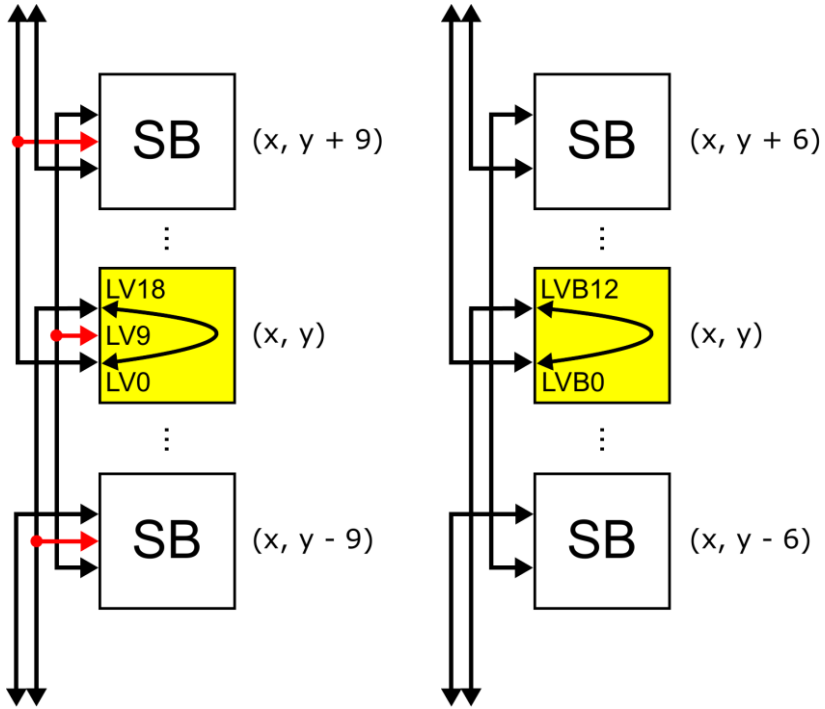
- Diagonal



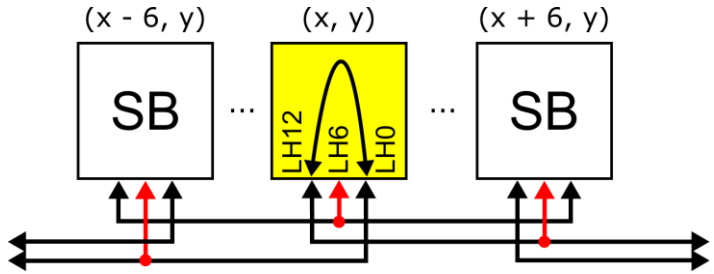
No directional bias, larger span for vertical wires

Long-Range Connections

- Vertical, LEN-18 and LEN-12



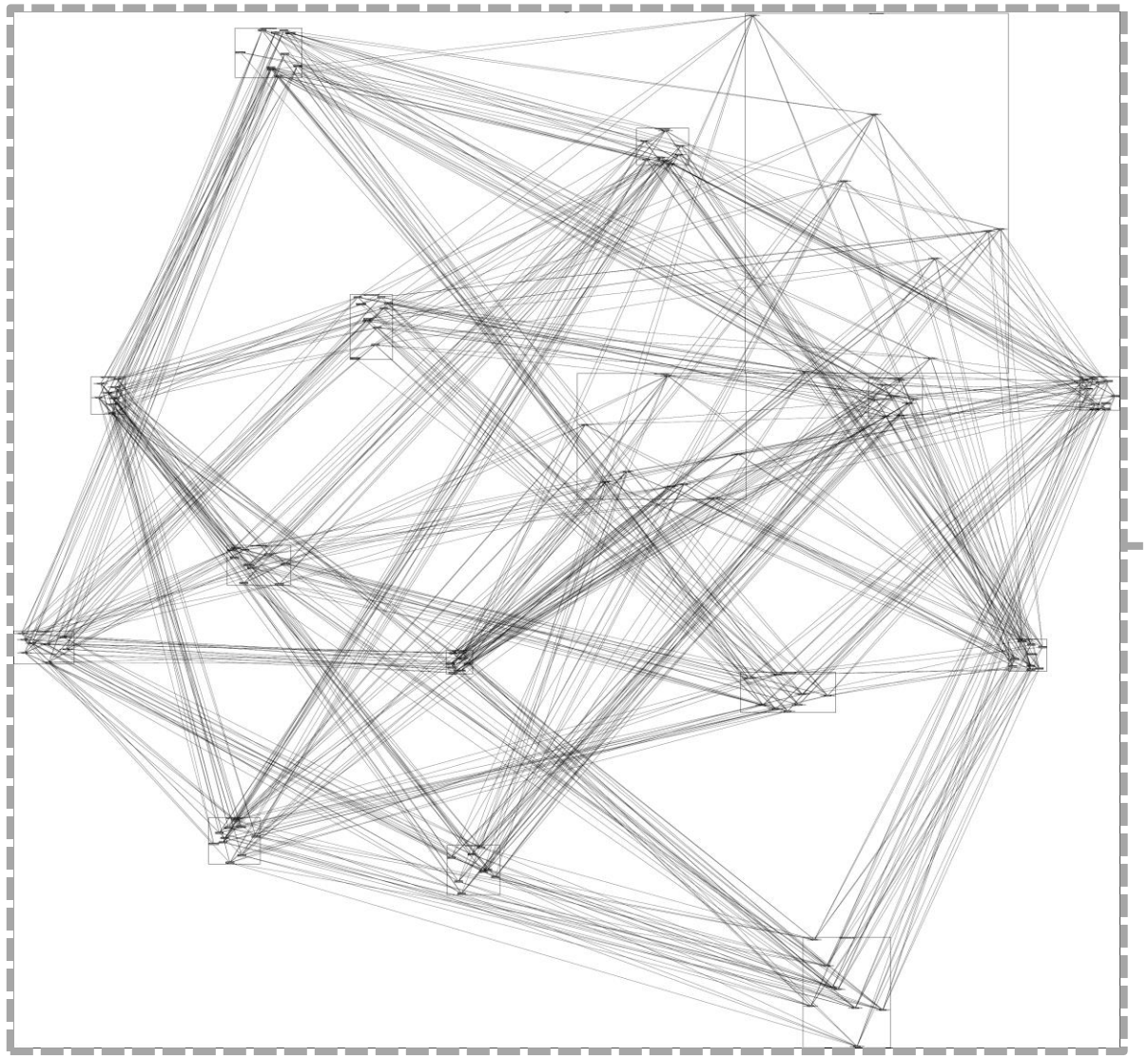
- Horizontal, LEN-12



Bidirectional, one tap midway, vertical L-12 for high speed signals

Adjacency Analysis

Adjacency Analysis with Clustering



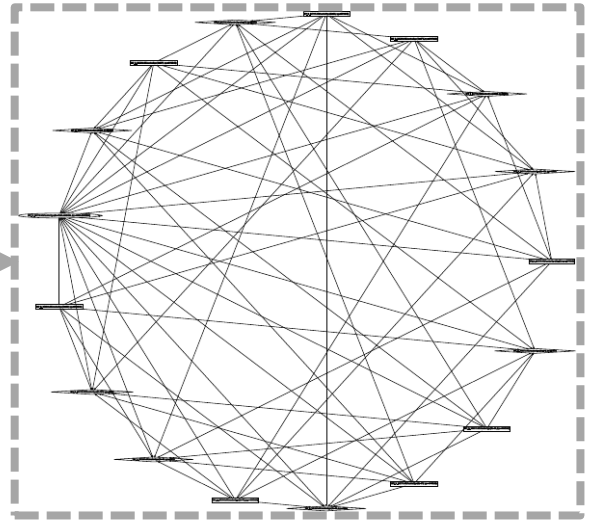
Input vendor-independent connectivity graph

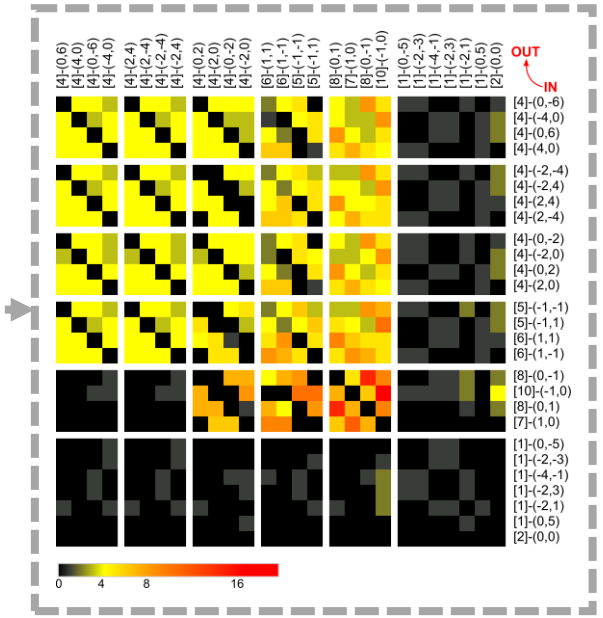
NetCracker

Adjacency pass and clustering by

- name or
- direction vector

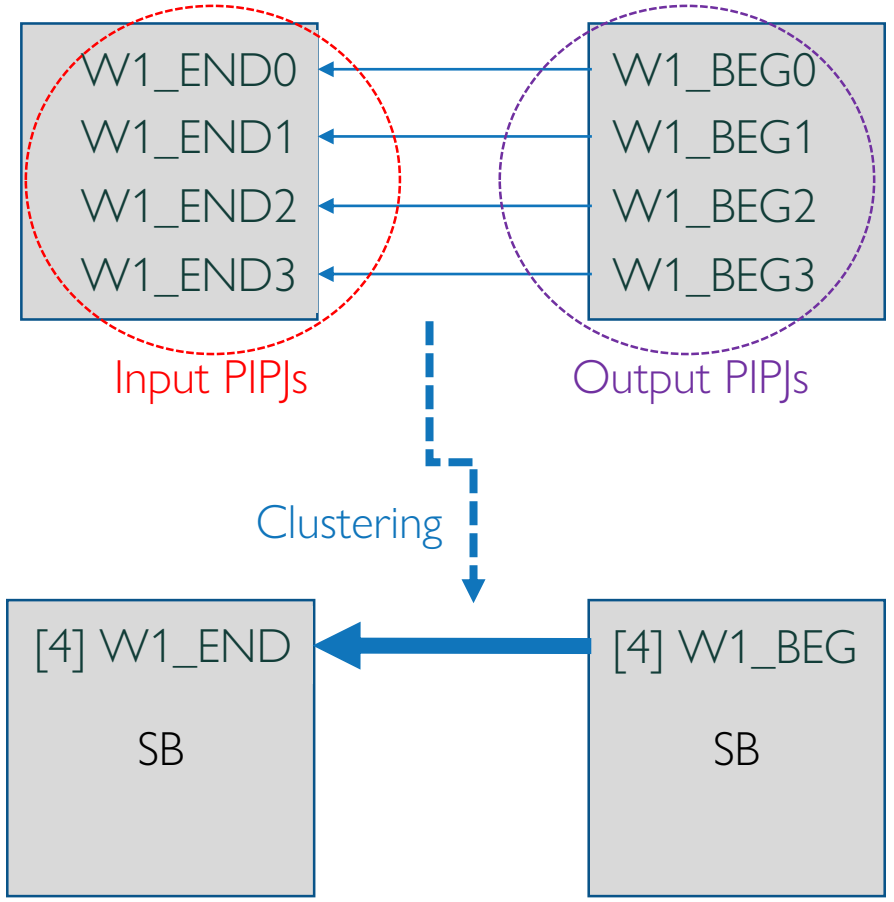
Connectivity subgraph





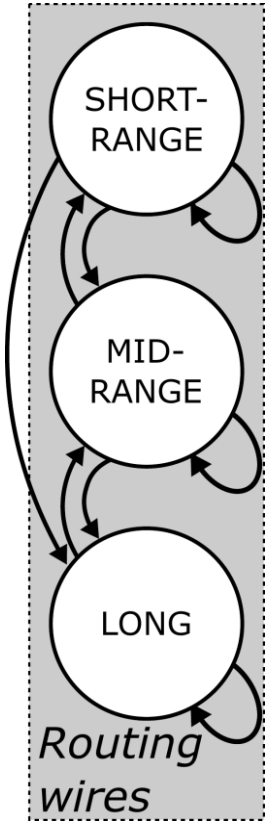
Adjacency heat map

PIPJ Clustering

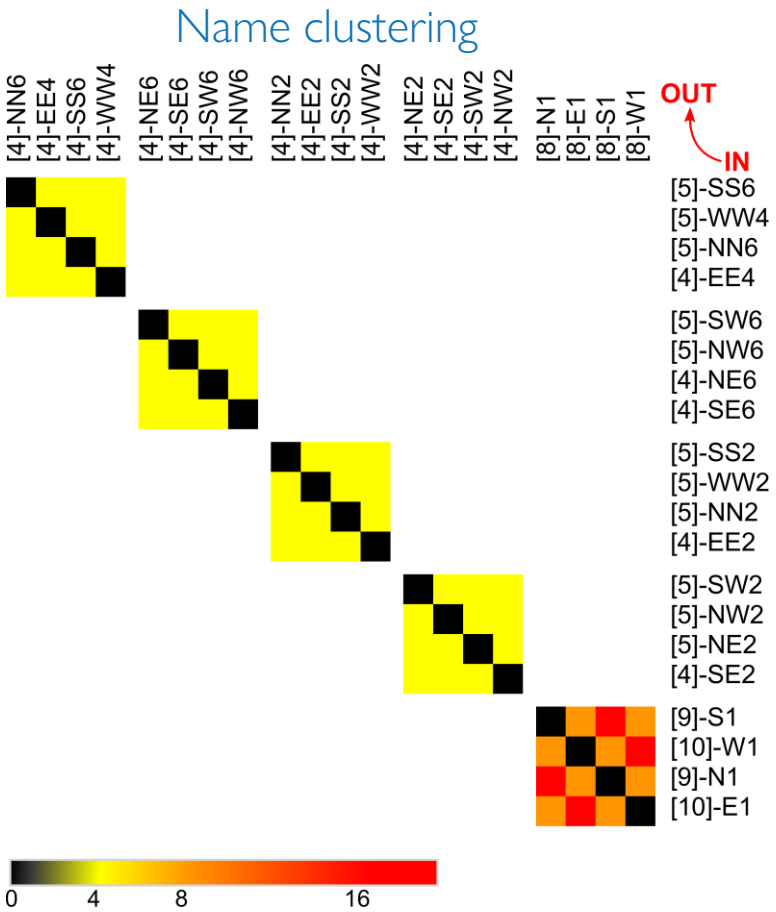


Clustering options: (1) by name and (2) by direction vector

Wire-to-Wire Adjacency Analysis



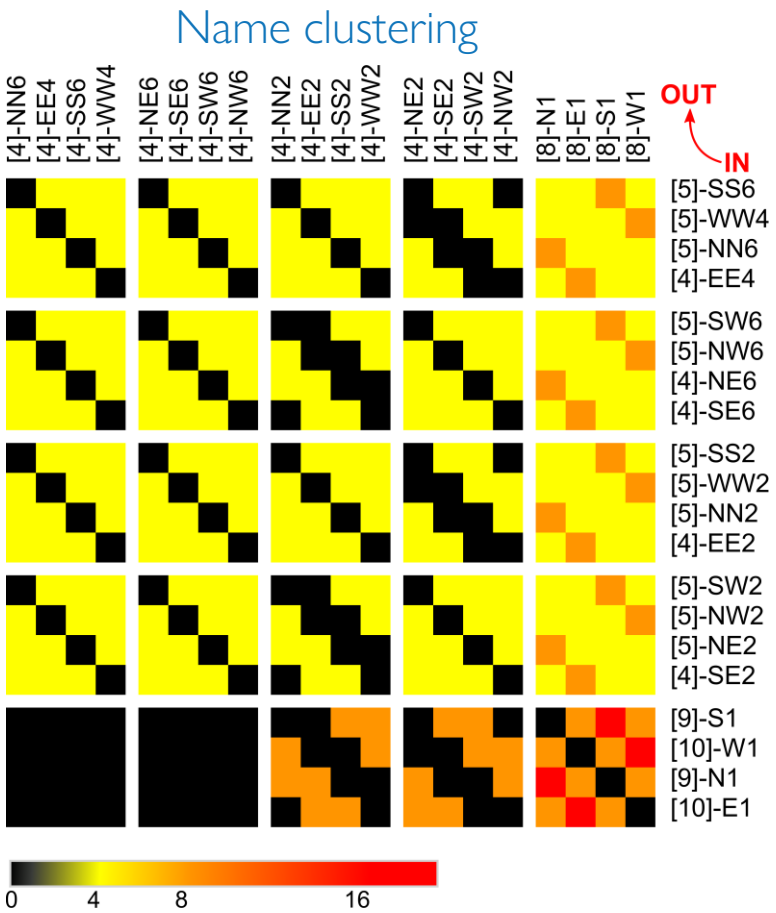
Short- and Mid-Range Adjacency Analysis



- Adjacency heat map
  - Rows: input PIPJs
  - Columns: output PIPJs
  - Inside brackets: cluster size
- Secondary destinations (stubs) included

Absence of U-turns

Short- and Mid-Range Adjacency Analysis

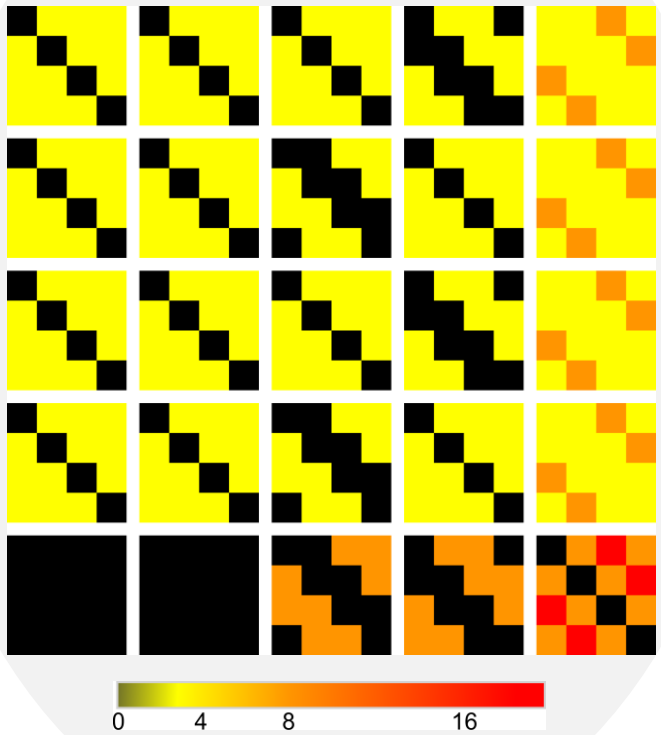


- LEN-1 do not drive LEN-4 and LEN-6
- Cardinal mid-range wires
  - do not drive LEN-2 returning to the half-plane of the source

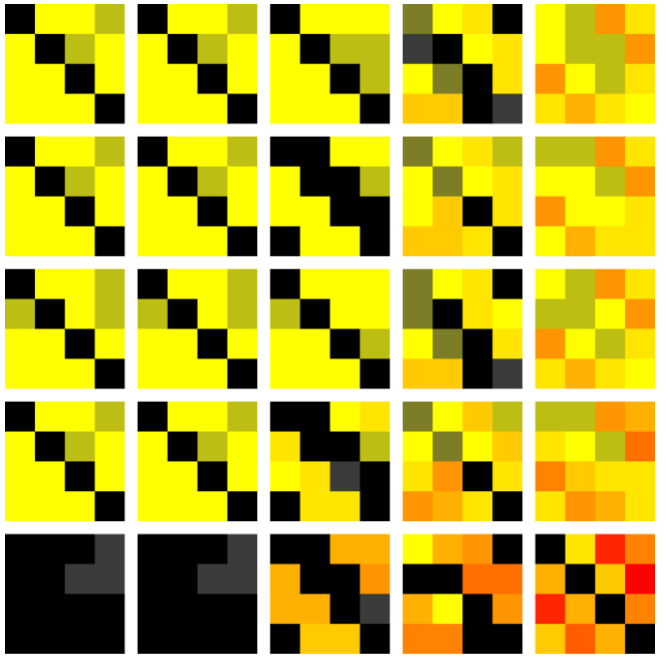
Number of wires each wire can drive vastly surpasses three

Short- and Mid-Range Adjacency Analysis

Name clustering



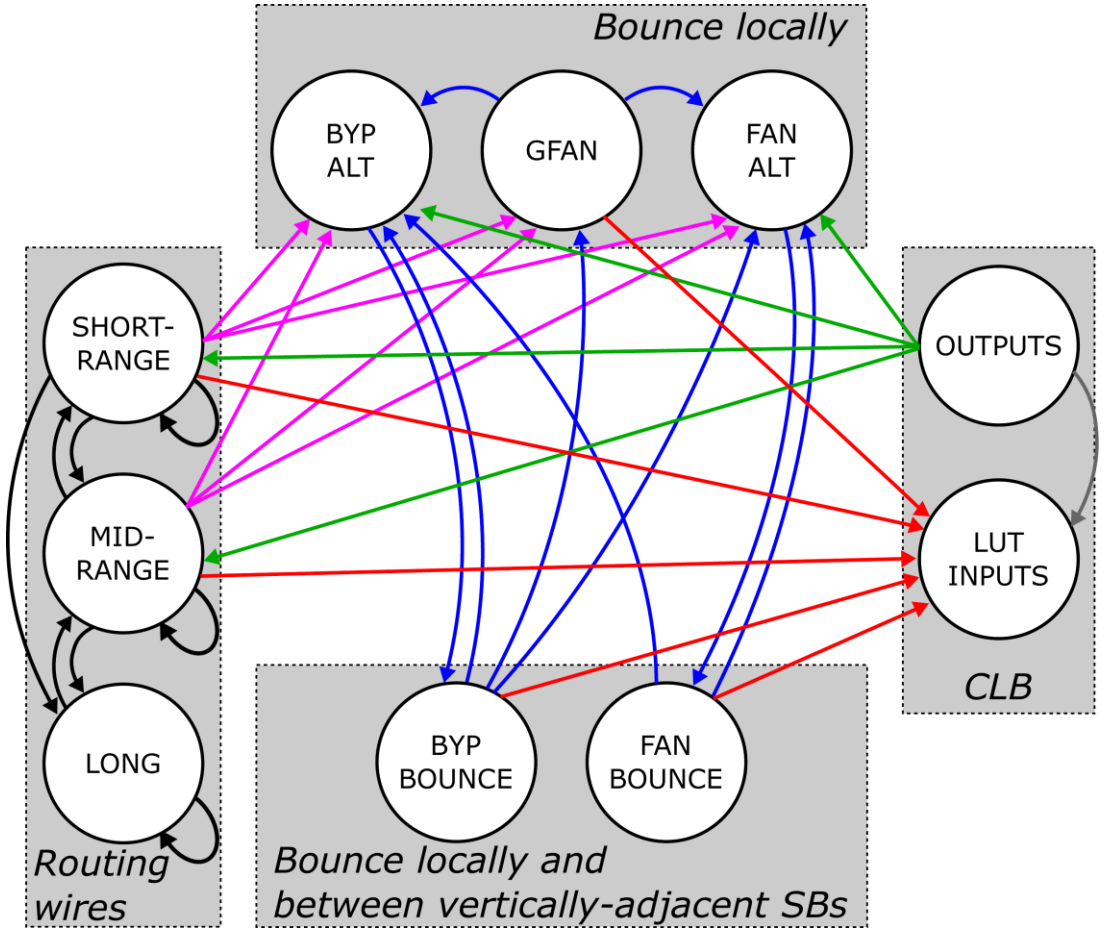
Direction-vector clustering



Not identical, but most of the regularity retained

The Full Picture

- Channel widths
- Wires to CLB inputs
- CLB outputs to wires and SBs
- Feedbacks: CLB to CLB
- **(New)** Bounce locally
- **(New)** Connections between vertically-adjacent SBs
- Routing MUX sizes



Understanding existing architectures is key for innovation

NetCracker

- Paper: https://doi.org/10.1145/3431920.3439285
- GitHub: https://github.com/mortbopet/netcracker
- Contact: mirjana.stojilovic@epfl.ch