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#### An Integrated Circuit Backside Approach for Large Area Deprocessing with Chemically Assisted Focused Ion Beam Sputtering and Optical Metrology Feedback

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## **Presentation Outline**

- Introduction
- Background
- Work Flow Description
- Selected Results from Chemically Assisted Argon Ion Delayering 14nm and 10nm devices
- Application development topics for Variolon
- Summary
- Published Work and References



#### Introduction

- Demonstrate results and methodology for large scale integrated circuit (IC) delayering of an advanced semiconductor fabrication nodes (14 & 10 nm) utilizing several focused ion beam circuit techniques such as chemically assisted material removal with integrated optical emission for layer detection and endpoint termination.
  - Backside Approach
    - Sample preparation involved
  - Scanning Argon Ion Beam (5 KeV or less)
  - Gas/Water Delivery Design
  - Ultraviolet (UV) photon based endpointing
    - Stand on the shoulders of giants
  - Based on original research from the IARPA Rapid Analysis of Various Emerging Nanoelectronics (RAVEN) Program.
  - Includes capabilities for substrate removal with XeF<sub>2</sub>, charge neutralization with an electron flood gun, and gas/leak detection with a RGA.



# Ion Beam Based IC Delayering

- There are a number of IC delayering techniques, but ion beam based techniques appear to be a larger area of focus for the most advanced IC manufacturing nodes. Advanced nodes can be considered 14 nm down to 2 nm (18A).
- For localized delayering xenon plasma FIBs systems are preferred for nanoprobing and failure analysis; for large area delayering broad beam argon ion systems have been developed.
- Delayering uniformity and stopping on the target layer are the key challenges, and various approaches have been investigated.



#### PLASMA FIB DEPROCESSING OF INTEGRATED CIRCUITS FROM THE BACKSIDE

E.L. Principe<sup>1</sup>, Navid Asadizanjani<sup>2</sup>, Domenic Forte<sup>2</sup>, Mark Tehranipoor<sup>2</sup>, Robert Chivas<sup>3</sup>, Michael DiBattista<sup>3</sup>, and Scott Silverman<sup>3</sup> <sup>1</sup>Synchrotron Research, Inc., Melbourne Beach, Fla. <sup>2</sup>Florida Institute for Cybersecurity, University of Florida, Gainesville, Fla. <sup>3</sup>Varioscale Inc., San Marcos, Calif. eprincipe@synchres.com

#### A Backside Approach

- There are multiple advantages of taking a backside approach for verification and validation activities. First layers are really easy access and image; the first layers are really important.
- Most Failure Analysis laboratories have the capability to back thin the silicon substrate for optical probing/FIB work.







Reliability of Ultra Thinning of Flip Chips for Through-Silicon Analyses



Chun-Cheng Tsuo<sup>\*</sup>, Erwan LeRov<sup>\*</sup>, Sambit Saha<sup>5</sup>, Lynnette Ansorge<sup>\*</sup>, Mark E. Potter<sup>\*</sup> <sup>\*</sup>Schlumherger Probe Systems, 150 Baytech Drive, San Jose, CA 95014 <sup>\*</sup>Agere Systems, 555 Union Boulevard, Allentowu, PA 18019

#### Intel Atom<sup>™</sup> 14nm Layer Structure

- The Intel Atom<sup>™</sup> was an advanced finfet transistor node. It has 9 metal layers in the IC. 10<sup>th</sup> Layer is a redistribution layer (RDL) for packaging.
- Interconnect layers M1 through M6 are all equal thickness at ~60nm.



7nm transistors from AMD are almost the same size as 14nm from Intel -World Today News (world-todaynews.com)



## Full Chip Imaging of the n-well Implants

- Once the device substrate is ultra-thinned, voltage contrast can be used to image the regions of n-well/p dopant with any electron microscope.
- Very useful for identifying the locations of PMOS and NMOS transistors in the device layout.
- Value in identifying some level of trojans if the n-well implant is missing. "Stealthy Dopant-Level Hardware Trojans", G.T. Becker et al. Proceedings of the 15th International Conference on Crytographic Hardware, Aug. 2013.

Dank field Optical Microscopy	Zeiss mSEM Single FOVs	Surface effect on SEM Voltage Contrast and Dopant Contrast, Li-
	n well	
	p substrate	
		HV mag det spot WD 1/14/20095 µm

#### **Removing Silicon: Stop on the STI Layer**

- We have engineered a reaction chamber to perform full die silicon substrate removal. The sample is loaded into the process chamber and the argon ion gun removes the native oxide.
- Then the sample is loaded into the load lock reaction chamber and XeF<sub>2</sub> etches the silicon substrate. Pressure is monitored to detect termination and chamber window shows the observable surface





#### **AFM Analysis of the Shallow Trench Isolation**

 The Shallow Trench Isolation (STI) layer is a homogeneous layer composed of silicon and oxygen, but it does contain topography as measured by AFM. The step height can be as deep as ~100 nm.





Height Sensor

1.0 µm

Height Sensor

2.0 µm

#### Scale of the Die Imaging to Transistor Optical to multiSEM zoom-in



#### **Optical Metrology for Layer Detection**

- The emission of characteristic photons occurs when the surfaces of metals, semiconductors, and glasses are bombarded by high energy ion species (argon, xenon, etc).
- First published work in 1973, "Photon Emission From Low-Energy Ion and Neutral Bombardment of Solids, N.H. Tolk *et al*, Bell Laboratories, N.J.
- The deceleration of the energetic species appears to be the mechanism responsible for photon emission. The mechanism is not fully understood. The effect has been shown to be enhanced by oxygen/water.
- For the IC materials of interest, the characteristic photons have ultraviolet wavelengths. Technique has obvious implications for material identification.



#### **High Observability**

#### **Operation Capabilities**

- Software enables control of major features such as argon ion source processing conditions, vacuum state, sample load and unload, and chemical delivery.
- Load lock (LL) allows for rapid exchange of samples in minutes.
- Navigation can be achieved with layout coordinates to target specific die locations during ion milling operations.





#### Ion induced UV Spectroscopy

 Using 1-2 uA Argon ion beam generates significant amounts of sputtered material and optical signal intensity.

Counts

Aluminum has a predominant peak at 395 nm



Wavelength (nm)

#### Ion induced UV Spectroscopy

- Copper has a predominant peak at 325 nm.
- This technique has • some differences over more traditional analytical analysis techniques such as EDS, SIMS, Auger, or **XPS.** Using optical detection allows us to work in high partial pressure of chemistry and still be surface sensitive to the nanometer level.



#### The Importance of Gas Delivery

Pc

- One of our key engineering investments was in developing and integrated a gas doser into the system.
- The difference between "injection" and "dosing" involves an effuser that can be used to target the surface and provide a level of directionality to improve efficiency.
- The water normalizes the sputter rate of materials like copper and silicon oxide so they are removed uniformly.
- Commonly used in Ultra High vacuum (UHV) work. The effuser is sized on the order of the full chip.





#### **Previous FIB-Circuit Edit Work**

- FIB circuit edit endpoint detection from 1998.
- Measured photons corresponds to the Aluminum photon intensity.
- Technique failed to be useful due to aspect ratio challenges. This is not an issue with the delayering application.



"Focused ion beam induced optical emission spectroscopy", B.W. Ward, JVST 1988

#### **Previous FIB-Circuit Edit Work (Part II)**

- MultiMode Imaging with OptiFIB with co-axial optical column.
- Images with reflected light, secondary electron, and impact generated UV photon emission.



OptiFIB Column

"Imaging and Material Analysis from Sputter-Induced Light Emission Using Coaxial Ion-Photon Column," C-c Tsao etalm, Microelectronics Reliablity, 2002

#### **Backside Delayering Metrology**

exposed.

 As the surface is sputtered while dosing with water, the signal on the silicon PMT initially increases as the STI layer is removed, and then decreases as the tungsten Metal 0 (M0) layer is



#### **Reaching the Metal 0 Surface on 14nm**

 The tungsten provides an excellent etch stop for the ion mill process. It sputters very slowly due to high Z, and density. This is an important reconstruction layer, and we reach it right after STI.

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#### **M0** Detail After Delayering

• Surface quality of the M0 layer is always very high. The water assisted process Linnin Helios 650 

#### 6 mm x 6 mm Layer Deprocessing

 'full chip' delayering stability of the system with a 6mm x 6 mm trench. The tool can operate overnight. Typically, each layer would be targeted, but layers can be skipped if multiple devices are available.





Varioscale, Inc.

## **Endpointing on Via0/Metal 1**

- Water dosing modulates the sputter rates of the materials.
- Beam shape is still under investigation. Beam tails play an important role in sputtering and signal generation.





## Via0/Metal 1 and Metal 1 Surfaces

- You can use chemically assisted argon ion sputtering to reach a Surface Uniformity better than 20nm on 5/ 7 /10/ 14 nm ICs
- Control material removal to the via layer for accurate 3D stitching of the IC information



#### M1 Example on 10nm

irrage\_Export\_3.bmp - IrfanView (Zoom: 35257 x 15861)

- 0 X



#### M3 Example on 10nm

#### CROW02 stitched data sets from a Zeiss mSEM



#### Summary

 A highly success approach using established FIB techniques including a backside approach, chemically assisted sputtering, optical endpointing.





# Thank You

#### **Variolon Features & Capabilities**

#### System Includes

- UHV vacuum system with integrated load lock
  - Base pressure 10<sup>-7</sup> torr
  - Operating pressure 10<sup>-5</sup> torr
- Argon/Xenon capable focused ion beam:
  - Typically 2 uA, Capable of 4 uA beam current
  - Full 10 mm x 10 mm scan range with electrostatic deflection
  - Modulated dwell time from 50 ms to 400 ms
  - Beam spot size 200 um at 33 mm
- 5 axis stage motion during deprocessing
  - Samples as large as 25 mm x 25 mm die
  - Capable of glancing angle sputtering
- Optical Metrology for layer detection of silicon and copper layers
- Integrated gas manifold and chemical delivery system
  - Holds water, Xef2, organic compounds
  - Additional slots available for customer development

# **Further Dev: Charge control**

 Remnants remain based on circuit architecture even with excess gas delivery.

Electron flood gun shall be used to improve delayering of specific circuits such as test chips.





#### **Surface Protection after Delayering**

- We have integrated a sputter target into the Variolon for surface layer protection.
- Typically using carbon since the next step in the workflow is SEM analysis.
- Other materials can be tested/investigated.



# **Application Dev: Contamination Removal**

- Develop software plotting routine that visualizes the locations and sizes of the contamination locations.
- Direct ion beam to remove contamination at the target locations.
- Rescan the surface to show the surface contamination has been removed (all blue)
- Look at optical component recovery (fibers/lenses) or space grade electron detectors.

#### Locations identified with target contaminate



# **Engineering Dev: Ultimate Sensitivity**

- We have the alpha system at Varioscale to test the sensitivity of the UV spectroscopy detection method.
- Several calibration samples under consideration.



# **Engineering Dev: Gas Flow Optimization**

- We currently deliver water vapor to the surface in excess. This effectively normalizes the sputter rate but slows down the material removal rate.
- We want to explore using MolFlow (CERN) to simulate the gas flow dynamics of the effuser and the surface coverage.



**MolFlow / SynRad documentation** 

# The Backside Delayering Concept

- This system is engineered for the task of full layer uniform delayering of advanced node integrated circuits using chemical assisted ion deprocessing.
- The Variolon integrates well established technologies from semiconductor circuit edit and failure analysis to create a novel IC delayering system
  - Photon based endpoint metrology
  - Integrated gas chemistries for uniformity
- The platform builds upon the existing VarioEdit & VarioMill software for faster adoption by experienced users.
- Tool platform provides expanded capabilities for materials analysis and spectroscopy (UV spectroscopy and mass spectrometry).



#### **Published Work on IC Delayering**

- Nicola Kovač, "Homogenous Delayering: A key challenge for successful reverse engineering", Fraunhofer Research Institute for Microsystems and Solid State Technologies EMFT, HARRIS Workshop @ Bochum, 24.-25.01.2023
- D. Douglass, K. Godin; "Whole-Chip Delayering for Failure Analysis and Quality Assurance." EDFA Technical Articles 1 May 2023; 25 (2): 4–8. doi: <u>https://doi.org/10.31399/asm.edfa.2023-2.p004</u>
- P. Nowakowski, M. Ray, P. Fischione and J. Sagar, "Top-down delayering by low energy, broad-beam, argon ion milling a solution for microelectronic device process control and failure analyses," 2017 28th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC), Saratoga Springs, NY, USA, 2017, pp. 95-101, <u>doi: 10.1109/ASMC.2017.7969206.</u>
- E.L. Principe, Navid Asadizanjani, Domenic Forte, Mark Tehranipoor, Robert Chivas, Michael DiBattista, Scott Silverman, Mike Marsh, Nicolas Piche, John Mastovich; "Steps Toward Automated Deprocessing of Integrated Circuits." Proceedings of the ISTFA 2017 Conference Proceedings from the 43rd International Symposium for Testing and Failure Analysis. Pasadena, California, USA. (pp. pp. 285-298). ASM. <u>https://doi.org/10.31399/asm.cp.istfa2017p0285</u>
- H. H. Yap, Z. J. Lau, "Delayering Techniques: Dry/Wet Etch Deprocessing and Mechanical Top-Down Polishing", Microelectronics Failure Analysis: Desk Reference, 7th ed., edited by Tejinder Gandhi, ASM International, 2019, p 379–390, <u>https://doi.org/10.31399/asm.tb.mfadr7.t91110379</u>

- K. S. Wills, S. Perungulam, "Delayering Techniques: Dry Processes, Wet Chemical Processing and Parallel Lapping," Microelectronics Failure Analysis Desk Reference, Sixth Edition, pp. 397-416. <u>http://dl.asminternational.org/istfa/proceedings-pdf/ISTFA2023/84741/550/662604/istfa2023p0550.pdf</u>
- A.G. Kimura, A.R. Waite, J. Scholl, G.D. Via; "Applied Failure Analysis Tools and Techniques Toward Integrated Circuit Trust and Assurance" EDFA Technical Articles 1 February 2021; 23 (1): 12–18. doi: <u>https://doi.org/10.31399/asm.edfa.2021-1.p012</u>
- Y. Patel, J. Baur, J. Scholl, A.R. Waite, A. Kimura, J. Kelley, R. Ott, G.D. Via; "A Sample Preparation Workflow for Delayering a 45 nm Node Serial Peripheral Interface Module". EDFA Technical Articles 1 November 2021; 23 (4): 4–13. doi: <u>https://doi.org/10.31399/asm.edfa.2021-4.p004</u>
- W. E. Vanderlinde, C. J. Von Benken, and A. R. Crockett, "Rapid integrated circuit delayering without grass", Proc. SPIE 2874, Microelectronic Manufacturing Yield, Reliability, and Failure Analysis II, (12 September 1996); <u>https://doi.org/10.1117/12.250834</u>
- R. Alvis, T. Landin, C. Rue, P. Carleson, O. Sidorov, A. Erickson, C. Chu, "Plasma FIB DualBeam Delayering for atomic force NanoProbing of 14 nm FinFET devices in an SRAM array." (2015). International Symposium for Testing and Failure Analysis. <u>https//doi:10.31399/asm.cp.istfa2015p0388</u>

- H. Y. Choi, S. J. Kim, C. H. Kang, C. C. Tsao, "A new Delayering application workflow in advanced 5nm technology device with xenon plasma focus ion beam microscopy." (2021). International Symposium for Testing and Failure Analysis. <u>doi:10.31399/asm.cp.istfa2021p0274</u>
  - E. Kim, J. Lee, J. Lee, "Plasma FIB Delayering and Nanoprobing with EBIRCH for localizing metal shorts in DRAM". (2021). International Symposium for Testing and Failure Analysis. doi:10.31399/asm.cp.istfa2021p0150

•

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- P. Nowakowski, M. Boccabella, M. Ray, P. Fischione; "Advances in Large-Area Microelectronic Device Deprocessing for Physical Failure Analyses and Quality Control." Proceedings of the ISTFA 2018. ISTFA 2018: Conference Proceedings from the 44th International Symposium for Testing and Failure Analysis. Phoenix, Arizona, USA. (pp. pp. 520-524). October 28–November 1, 2018. ASM. <u>https://doi.org/10.31399/asm.cp.istfa2018p0520</u>
- P. Nowakowski, C. Bonifacio, M. Ray, P. Fischione, "Large area semiconductor device delayering for failure identification and analyses". ISTFA Conference proceedings from the 47th international symposium for testing and failure analysis (pp. 410-413). ASM International.
- Y. Patel, J. Scholl, A.R. Waite, A. Kimura, J. Kelley, A. Kimura, R. Ott, and G.D. Via; "A Comparative Analysis of Broad and Focused Ion Beam Techniques for Backside Material Removal of a 14 nm FinFET Device". EDFA Technical Articles 1 November 2021; 23 (4): 4–13. doi: <u>https://doi.org/10.31399/asm.edfa.2021-4.p004</u>

- D. Zudhistira, V. Viswanathan, V. Narang, J.M. Chin, S. Sharang, K. Novotny, J. Vincen Oboňa; "Precision Xe Plasma FIB Delayering for Physical Failure Analysis of Sub-20 nm Microprocessor Devices." Proceedings of the ISTFA 2017. ISTFA 2017: Conference Proceedings from the 43rd International Symposium for Testing and Failure Analysis. Pasadena, California, USA. (pp. pp. 574-579). ASM. https://doi.org/10.31399/asm.cp.istfa2017p0574
- D. Zhang, G. Van Der Wal, P. Miller, D. Stoker, E. Matlin, N. Marri, G. Gan, J. Zhang, J. Asmuth, S. Chai, D. Weaver, M. Piacentino, S. Silverman, M. DiBattista, R. Chivas, C. G. L. Ferri, D. Taylor, J. Furlong, T. Harper, D. Kobs, "Fast, Full Chip Image Stitching of Nanoscale Integrated Circuits" GoMATech 2019
- P. Nowakowski, J. Liu, M. Boccabella, M. Ray, P. Fischione, "An innovative technique for large-scale Delayering of semiconductor devices with nanometric-scale surface flatness". International Symposium for Testing and Failure Analysis. (2022). doi:10.31399/asm.cp.istfa2022p0414
- Y. Patel, J Scholl, A.R. Waite, J. Kelly, A. Kimura, R. Ott, GD Via, "A comparative Analysis of Broad and Focused Ion Beam Techniques for Backside, Material removal of a 14 nm node FinFET device",Government microcircuit and critical technology conference, GoMATech 2023
- A.R. Waite, Y. Patel, J. J. Kelley; J. H. Scholl; J. Baur; A. Kimura, "Preparation, Imaging, and Design Extraction of the Front-End-of-Line and Middle-of-Line in a 14 nm Node FinFET Device", 2021 IEEE Physical Assurance and Inspection of Electronics (PAINE)

- A. Crockett, M. Almoustafa and W. Vanderlinde, "Plasma delayering of integrated circuits," in Microelectronics Failure Analysis: Desk Reference, 5 ed., EDFAS Desk Reference Committee, Ed., Materials Park, OH: ASM International, 2004, pp. 464-472.
- M. DiBattista, H. Beaulieu, R. Chivas, J. Sheeder, S. Silverman, "Advantages of Chemically Assisted Argon Focused Ion Beam Processing for Full Chip Delayering Requirements," 16<sup>th</sup> FIB –SEM User Group Meeting, May 22 – May 23, 2024, Kossiakoff Center, Laurel Maryland.
- M. DiBattista, H. Beaulieu, R. Chivas, J. Sheeder, S. Silverman, "Large Area Circuit Delayering from the Backside Using Chemically assisted Focused Ion Beam Sputtering with Optical Metrology Feedback" Proceedings of the ISTFA 2024. ISTFA 2024: Conference Proceedings from the 50th Symposium for Testing and Failure Analysis. San Diego, California, USA.
- N. Padro, T. Balint, N. Harner, J. Scholl, Y. Patel, M. Sale, A. Kimuar, "A Quantitative and Automated Quality Metric for Delayering Integrated Circuits", Proceedings of the ISTFA 2024. ISTFA 2024: Conference Proceedings from the 50<sup>th</sup> Symposium for Testing and Failure Analysis. San Diego, California, USA. (pp. pp. 363-367).
- M. DiBattista, H. Beaulieu, R. Chivas, J. Sheeder, S. Silverman, "Full Chip Backside Delayering of 10 nm Node Integrated Circuits with Chemically Assisted Focused Ion Beam Deprocessing" EDFA Technical Articles, 15 January 2025, *in press*